UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.: 2933SE-85

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Express Mail Label No.: IB914615988

Title: "METHOD AND APPARATUS FOR DRIVING SOLID STATE IMAGE SENSOR"

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

Enclosed for filing with the above-identified utility patent application, please find the following:

1. [X] Specification (Total Pages of Text, including Abstract and Claims: 18)
2. [X] Drawing(s) (35 USC 113) (Total Sheets: 5) [X] FORMAL [] INFORMAL
3. [X] Combined Declaration and Power of Attorney (Total Pages: 3) [X] Signed [] Unsigned
4. [X] Assignment Papers *(cover sheet & document(s))*
5. [X] Return Postcard (MPEP 503) *(should be specifically itemized)*
6. [X] A check in the amount of $760.00 is enclosed.

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	(COL. 1) NO. FILED			(COL. 2*) NO. EXTRA	SMALL ENTITY			LARGE ENTITY	
					RATE	FEE		RATE	FEE
BASIC FEE:						$380.00	OR		$760.00
TOTAL CLAIMS:	7	-	20	0	X $9 =		OR	X $18 =	$0.00
INDEP. CLAIMS:	2	-	3	0	X $39 =		OR	X $78 =	$0.00
____ MULTIPLE DEPENDENT CLAIMS					+ $130 =		OR	+$260 =	$0.00
*IF THE DIFFERENCE IN COL. 2 IS LESS THAN ZERO, ENTER "O" IN COL. 2.					TOTAL:				$760.00

OTHER INFORMATION:

1. [X] The Commissioner is hereby authorized to debit any underpayments or credit any overpayment to Deposit Account No. 19-1970.

2. [X] The Commissioner is hereby authorized to charge all required fees for extensions of time under §1.17 to Deposit Account No. 19-1970.

3. [X] Foreign Priority benefits are claimed under 35 USC §119 of Japanese Patent Application Serial No. 10-305820 filed October 27, 1998.

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Respectfully Submitted,

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METHOD AND APPARATUS FOR DRIVING SOLID STATE IMAGE SENSOR

BACKGROUND OF THE INVENTION

The present invention relates to a method and apparatus for driving a solid state image sensor which operates an electronic shutter.

An image sensing apparatus which has a solid state image sensor, like a CCD (Charge Coupled Device), controls the exposure of the solid state image sensor to achieve an optimal exposure state. This exposure control uses an iris mechanism which mechanically controls the amount of incident light to the solid state image sensor in accordance with the luminance of light reflected from a target object. Alternatively, the exposure control can use a so-called electronic shutter which controls the period the solid state image sensor accumlates a charge in accordance with the luminance of light reflected from the target object. The solid state image sensor has light-receiving pixels arranged in a matrix form, which stores (accumlates) information charges that are generated in accordance with the incident light.

Fig. 1 is a block diagram showing the structure of a prior art solid state image sensor, and Fig. 2 is a timing chart showing the operation of the prior art solid state image sensor. Referring to Fig. 1, a frame transferring type CCD solid state image sensor 1 includes a light-receiving section 1i, a storing section 1s, a horizontal transferring section 1h, and an output section 1d. The light receiving section 1i has a plurality of parallel transfer registers arranged continuously in the vertical

direction. A plurality of light-receiving pixels are formed by each bit of the transfer registers. When the light from a target object irradiates the light-receiving pixels, each light-receiving pixel generates and stores a charge corresponding to the image of the target object. The storing section 1s has a plurality of transfer registers continuing from the transfer registers of the light-receiving section 1i. The number of bits of each transfer register of the storing section 1s is the same as that of each transfer register (shift register) of the light-receiving portion 1i. The storing section 1s temporarily stores information charges corresponding to a single display image output by the light-receiving section 1i. The horizontal transfer section 1h has a single horizontal transfer register. Each bit of the horizontal transfer register is connected to the transfer registers of the storing section 1s. The horizontal transfer section 1h receives the stored information charges, which correspond to the display image, from the storing section 1s in units of single lines and sequentially transfers the single line units to the output section 1d. The output section 1d has an electrically independent capacitor and an amplifier, which eliminate potential changes at the output section 1d. The output section 1d receives the information charges serially from the horizontal transfer section 1h in single line units and converts the information charges to a voltage value and then outputs an image signal Y(t).

A clock generator 2 generates a multi-phase vertical transfer clock φv, a storage transfer clock φs, and a horizontal transfer clock φh in response to horizontal and vertical timing signals HT, VT. The vertical transfer clock φv is sent to the light-receiving section 1i of the solid state image sensor 1, the storage transfer clock φs is sent

to the storage section 1s, and the horizontal transfer clock ϕh is sent to the horizontal transfer section 1h.

When the light-receiving section 1i receives the vertical transfer clock ϕv, the stored information charges in each light-receiving pixel of the light-receiving section 1i are transferred to the storage section 1s. This is the vertical scanning return period. When the storage section 1s receives the storage transfer clock ϕs, the information charges transferred from the light-receiving section 1i in accordance with the vertical transfer clock ϕv are acquired by the storage section 1s. Additionally, the acquired information charges are transferred to the horizontal transfer section 1h one line at a time. The information charges transferred to the horizontal transfer section 1h one line at a time in accordance with the storage transfer clock ϕs are further transferred to the output section 1d, sequentially. The clock generator 2 also generates a substrate clock ϕb which rises for a predetermined time period in response to a discharge timing signal BT. The substrate clock ϕb is applied to the substrate side of the solid state image sensor 1. When the substrate clock ϕb is active, the information charges stored in the light-receiving pixels of the light-receiving section 1i are discharged toward the substrate side. Since the vertical transfer clock ϕv falls synchronously with the rising of the substrate clock ϕb, the discharge of information charges toward the substrate is smooth.

In this manner, information charges are stored in each light-receiving pixel of the light-receiving section 1i during a period L, which starts from when the discharge of information charges in accordance with the substrate clock

ϕb is completed to when transmission is commenced by the vertical transfer clock ϕv. The stored period of the information charges, or the shutter speed, is controlled by adjusting the timing of the substrate clock ϕb.

A timing controller 3 generates the vertical timing signal VT and the horizontal timing signal HT from a reference clock CK, which has a constant cycle, and sends the signals VT, HT to the clock generator 2. If, for example, the NTSC standard is employed, the timing controller 3 causes the horizontal timing signal HT to rise each time 910 reference clocks CK, which frequency is 14.32 MHz, are counted. The timing controller 3 also causes the vertical timing signal VT to fall each time 525/2 horizontal timing signals HT are counted. The timing controller 3 also causes the discharge timing signal BT to rise during the vertical scanning period based on exposure data indicating the exposure level of the solid state image sensor 1. The timing controller 3, for example, determines whether or not the exposure data, which is obtained by integrating the image signal Y(t) for every single display image unit, is within an optimal range. If the exposure data exceeds the exposure range, the rising timing of the pulse signals is delayed to shorten the storage period L of the information charges. On the other hand, if the exposure data has not yet reached the optimal level, the timing controller 3 advances the rise timing of the pulse signals to prolong the storage period L of the information charges.

The image sensor maintains the image signal Y(t) at an optimal level by changing the length of the period L, during which information charges are stored in the light-receiving section 1i, in accordance with the level of the image signal Y(t).

Fig. 3 is a cross-sectional view showing the light-receiving section 1i of a CCD solid state image sensor which employs a vertical overflow drain structure to absorb excess information charges on the substrate side. A diffusion region (P-well region) 12 having a P type conductivity is formed on the surface region of a semiconductor substrate 11 which has an N type conductivity and where a drain region is to be formed. Formed on the surface of this P-well region 12 is a diffusion layer (buried layer) 13 which has an N type conductivity and where a channel region is to be formed. The buried layer 13 is formed so as to be defined by an isolation region (not shown) on the surface of the P-well region 12 and to extend in one direction. First gate electrodes 15 are arranged at given intervals on the buried layer 13 via an insulating layer 14, and second gate electrodes 16 are arranged between the adjoining first gate electrodes 15 in such a way as to partially cover the first gate electrodes 15. The first and second gate electrodes 15, 16 are respectively supplied with four phase vertical clocks ϕv ($\phi v1$-$\phi v4$), each of which has a phase difference of 90 degrees from one to another and are synchronous with a vertical sync signal VD. The semiconductor substrate 11 is supplied with the substrate clock ϕb. A ground voltage is applied to the P-well region 12. The peak values of the vertical clocks $\phi v1$-$\phi v4$ and the substrate clock ϕb, or the potentials at the gate electrodes 15, 16 and the semiconductor substrate 11, are set based on the P-Well region 12.

In the vertical overflow drain structure, when the light-receiving section 1i stores information charges, the substrate clock ϕb is kept low, and one to three of the vertical clocks ($\phi v1$-$\phi v4$) are kept high. This selectively activates the first and second gate electrodes 15, 16. In

the part of the light-receiving section 1i where the first and second gate electrodes 15, 16 are activated, as shown in Fig. 4, a potential well (depletion layer) is formed near the buried layer 13. Accordingly, information charges are stored in the region from within the buried layer 13 to the surface of the P-well region 12. In the part of the light-receiving section 1i where the first and second gate electrodes 15, 16 are deactivated, a potential well is not formed in the buried layer 13 but a potential barrier for defining the light-receiving pixels is formed in the buried layer 13.

During the shutter operation for discharging the information charges stored in each of the light-receiving pixels, all of the vertical clocks $\phi v1$-$\phi v4$ are kept low and the substrate clock ϕb rises. Consequently, the potential well in the buried layer 13 becomes shallower while the potential well in the semiconductor substrate 11 becomes deeper. As a result, the potential barrier in the P-well region 12 disappears as indicated by the broken line in Fig. 4. In this manner, the information charges stored in the potential well in the buried layer 13 are moved to the semiconductor substrate 11 from the buried layer 13 along the potential profile and are discharged therefrom.

In the solid state image sensor 1 having the vertical overflow drain structure, the output section 1d and the light receiving section 1i are formed on the same substrate. Thus, the substrate clock ϕb affects the output portion 1d during the shutter operation. Accordingly, the rise timing of the substrate clock ϕb is set within the horizontal scanning return period in order to prevent noise from being mixed with the image signal Y(t) acquired from the output portion 1d. However, the horizontal scanning return period

is very short, lasting only a few microseconds. Hence, if charges are stored in a large number of light-receiving pixels, all of the unnecessary charges in the light-receiving pixels may not be discharged and may thus remain in the light receiving pixels as residual charges. The residual charges may mix with the subsequently stored information charges and decrease the quality of the replayed display image.

SUMMARY OF THE INVENTION

Accordingly, it is an objective of the present invention to provide a method and apparatus for driving a solid state image sensor which completely discharges unnecessary charges during the shutter operation.

To achieve the above objective, the present invention provides a method for driving a solid state image sensor that obtains image signals in display image units. The solid state image sensor includes a semiconductor substrate and a semiconductor layer formed on the semiconductor substrate. The semiconductor layer has an opposite conductivity to the semiconductor substrate. The semiconductor layer has a plurality of parallel channel regions arranged therein. A plurality of transfer electrodes are arranged on the semiconductor substrate. Each transfer electrode intersects the plurality of channel regions. Each of the channel regions generates and accumulates information charges. The driving method includes the steps of accumulating information charges in the channel region that correspond to a transfer electrode selected by selectively activating the plurality of transfer electrodes at a predetermined timing during a vertical scanning return period, transferring the accumulated

information charges to a transfer register, discharging the information charges in the channel regions toward the semiconductor substrate by keeping the plurality of transfer electrodes deactivated and increasing the potential at the semiconductor substrate, and repetitively executing the accumulating, transferring, and discharging steps to continuously obtain the image signals in display image units.

In a further aspect of the present invention, the present invention provides an apparatus for driving a solid state image sensor that obtains image signals in display image units. The solid state image sensor includes a semiconductor substrate and a semiconductor layer formed on the semiconductor substrate. The semiconductor layer has an opposite conductivity to the semiconductor substrate. The semiconductor layer has a plurality of parallel channel regions arranged therein. A plurality of transfer electrodes are arranged on the semiconductor substrate. Each transfer electrode intersects the plurality of channel regions. Each of the channel regions generates and accumulates information charges. The driving apparatus includes a timing controller for generating a predetermined timing signal based on a reference clock signal, and a clock generator for generating a vertical clock signal and a substrate clock signal based on the timing signal and applying the vertical clock signal and the substrate clock signal to the solid state image sensor. The clock generator activates the vertical clock signal so that the transfer electrodes are selectively activated and the information charges are accumulated in the channel regions corresponding to the activated transfer electrode, and deactivates the vertical clock signal so that the transfer electrodes are maintained in a deactivation state after transfering the

stored information charges. The the clock generator further activates the substrate clock signal so that the potential of the semiconductor substrate is increased and the information charges in the channel region are discharged when the transfer electrode is deactivated.

Other aspects and advantages of the present invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention that are believed to be novel are set forth with particularity in the appended claims. The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

Fig. 1 is a block diagram showing an image apparatus employing a prior art solid state image sensor;

Fig. 2 is a timing chart illustrating the operation of the image apparatus of Fig. 1;

Fig. 3 is a cross-sectional view showing a light-receiving section of a prior art solid state image sensor having a vertical overflow drain structure;

Fig. 4 is a diagram showing potential changes in the solid state image sensor of Fig. 3 in the vertical direction;

Fig. 5 is a timing chart illustrating a method for

driving a solid state image sensor according to the present invention;

Fig. 6 is a diagram showing potential changes when employing the solid state image sensor driving method according to the present invention;

Fig. 7 is a flowchart illustrating the method for driving the solid state image sensor; and

Fig. 8 is a schematic block diagram of a timing control circuit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reffering to Fig. 8, a clock generator 20 and a timing controller 30 are shown. The timing controller 30 receives a reference clock signal CK and generates predetermined timing signals (horizontal timing signal HT, vertical timing signal VT and discharge timing signal BT) based on the reference clock signal CK. The clock generator 20 generates a vertical transfer clock ϕv, a storage transfer clock ϕs, and a horizontal transfer clock ϕh based on the timing signals HT, VT. The clock generator 20 sends the vertical transfer clock ϕv and the horizontal transfer clock ϕh to the solid state image sensor. The clock generator 20 also generates a substrate clock signal ϕb in responce to the discharge timing signal BT. The timing controller 30 also causes the discharge timing signal BT to rise during the vertical scanning period based on exposure data indicating the exposure level of the solid state image sensor.

A method for driving a solid state image sensor according to the present invention will now be described

with reference to Figs. 5 to 7. The structure of the solid state image sensor is essentially the same as that of the prior art image sensor shown in Fig. 1, except that the control signals or clocks generated by the timing controller 3 and the clock generator 2 are activated as described below.

In the driving method according to the present invention, the frame transfer type solid state image sensor first keeps the transfer electrodes, which form the light-receiving pixels, deactivated and discharges the residing charges. The electronic shutter operation then discharges substantially all of the residing information charges. The transfer electrodes are then activated to store new information charges. In other words, when the transfer electrodes are activated in the frame transfer type solid state image sensor, a potential well is formed in the channel region below the transfer electrodes so that the functions of the light-receiving pixels become effective. The light-receiving pixels function effectively only during the storage period L of the information charges.

The transfer output of the information charges from the light-receiving section to the storage section, or the frame transfer is set during the blanking period of the vertical sync signal VD. After the frame transfer is completed, the four phase vertical clocks $\phi v1$-$\phi v4$ are fall, which deactivates all of the transfer electrodes. In this state, the substrate clock ϕb is fixed to the low level. This state is maintained until a shutter trigger ST rises. The timing of the shutter trigger ST is set based on the exposure level of the image sensor, or the exposure information indicating the average level of the image signal output by the image sensor, in the same manner as the prior

art solid state image sensor shown in Fig. 4.

As shown in Fig. 5, when the shutter trigger ST rises during the vertical scanning period, the substrate clock ϕb rises. This discharges the information charges residing in the channel region below the transfer electrodes toward the substrate. The substrate clock ϕb remains high over a predetermined period. Unnecessary residual information charges are discharged during this period. Among the four phase vertical transfer clocks $\phi v1$-$\phi v4$, for example, the first phase and second phase clocks $\phi v1$, $\phi v2$ rise synchronously with the falling of the substrate clock ϕb. This forms the potential well below the transfer electrodes to which the vertical transfer clocks $\phi v1$, $\phi v2$ are applied. The potential barrier is formed below the transfer electrodes to which the vertical transfer clocks $\phi v3$, $\phi v4$ are applied. The rise and fall timing of each vertical transfer clock is set within the horizontal scanning return period to prevent noise from mixing with the image signal.

The information charges generated by photoelectric conversion in the channel region are stored in the potential well. The accumulation of the information charges is maintained during the blanking period of the vertical sync signal VD until the frame transfer is commenced. Accordingly, the information charges generated in the channel regions are stored in the potential well during the period L from when the first and second phase clocks $\phi v1$, $\phi v2$ rise to when the frame transfer is commenced.

As shown in Fig. 6A, the preferred drive method substantially prevents the formation of the potential well in the channel region during the period from when the frame transfer is completed to when the storage of the information

charges is commenced. Thus, even if incident light in the channel region generates information charges, most of those charges are discharged toward the substrate side. As a result, only the subtle amount of charges residing in the channel region need be discharged toward the substrate side when the substrate clock ϕb rises to start the shutter operation. Accordingly, substantially all of the unnecessary information charges residing in the channel region are discharged even if the shutter operation is fast. This prevents unnecessary information charges from residing in the channel region. Furthermore, since the amount of charges discharged during the shutter operation is small, the charges are discharged sufficiently even if the potential of the substrate clock ϕb is low.

In the vertical overflow drain structure solid state image sensor of the preferred embodiment, the discharge of unnecessary charges is completed within a short period of time and unnecessary charges are thus prevented from residing in the channel region when the shutter operation is performed. Furthermore, the small amount of charges that are discharged during the shutter operation allows the voltage required for the shutter operation to be set at a low value. This decreases power consumption.

In the preferred embodiment, all of the transfer electrodes remain deactivated from when the frame transfer is completed to when the storage of the information charges is commenced in order to prevent the formation of the potential well in each channel region. Thus, the charges generated in the channel regions are discharged toward the substrate regardless of the intensity of the incident light at the channel regions. In other words, all of the charges in the channel regions are easily discharged toward the

semiconductor substrate when the potential at the semiconductor substrate increases.

The preferred embodiment employs four phase vertical transfer clocks. However, three phase or five phase transfer clocks may be employed.

It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.

WHAT IS CLAIMED IS:

1. A method for driving a solid state image sensor that provides image signals in display image units, wherein the solid state image sensor includes a semiconductor substrate, a semiconductor layer formed on the semiconductor substrate and having an opposite conductivity to the semiconductor substrate, the semiconductor layer having a plurality of parallel channel regions arranged therein, and a plurality of transfer electrodes arranged on the semiconductor substrate each intersecting the plurality of channel regions, wherein each of the channel regions generates and accumulates information charges, the driving method comprising the steps of:

storing information charges in the channel region that correspond to a transfer electrode selected by selectively activating the plurality of transfer electrodes at a predetermined timing during a vertical scanning period;

transferring the stored information charges to a transfer register;

discharging the information charges in the channel regions toward the semiconductor substrate by keeping the plurality of transfer electrodes deactivated and increasing the potential at the semiconductor substrate; and

repetitively executing the storing, transferring, and discharging steps to continuously obtain the image signals in display image units.

2. The driving method according to claim 1, wherein the potential at the semiconductor substrate is raised just before the next storing step.

3. The driving method according to claim 1, wherein a potential well having a predetermined depth is formed in the

selected channel region during the storing step to store the information charges.

4. The driving method according to claim 3, wherein the potential well is prevented from being formed in the discharging step.

5. An apparatus for driving a solid state image sensor that provides image signals in display image units, wherein the solid state image sensor includes a semiconductor substrate, a semiconductor layer formed on the semiconductor substrate and having an opposite conductivity to the semiconductor substrate, the semiconductor layer having a plurality of parallel channel regions arranged therein, and a plurality of transfer electrodes arranged on the semiconductor substrate each intersecting the plurality of channel regions, wherein each of the channel regions generates and accumulates information charges, the driving apparatus comprising:

a timing controller for generating a predetermined timing signal based on a reference clock signal; and

a clock generator for generating a vertical clock signal and a substrate clock signal based on the timing signal and applying the vertical clock signal and the substrate clock signal to the solid state image sensor, wherein the clock generator activates the vertical clock signal so that the transfer electrodes are selectively activated and the information charges are accumulated in the channel regions corresponding to the activated transfer electrode, and deactivates the vertical clock signal so that the transfer electrodes are maintained in a deactivation state after transfering the stored information charges, and wherein the the clock generator activates the substrate clock signal so that the potential of the semiconductor

substrate is increased and the information charges in the channel region are discharged when the transfer electrode is deactivated.

6. The driving apparatus according to claim 5, wherein the clock generator activates the substrate clock signal to raise the potential at the semiconductor substrate except when the information charges are stored.

7. The driving apparatus according to claim 5, wherein the clock generator keeps the substrate clock signal deactivated to keep the plurality of transfer electrodes deactivated except when the information charges are stored.

ABSTRACT OF THE DISCLOSURE

An image sensing device includes a solid state image sensor, such as a CCD. An electronic shutter controls the exposure of the sensor to light, and thus the period during which the sensor collects or accumulates an information charge with light receiving pixels. The image sensor includes a semiconductor substrate, a semiconductor layer having parallel channel regions formed on the substrate, and transfer electrodes which intersect the channel regions. The channel regions generate and store the information charges.

Fig.1 (Prior Art)

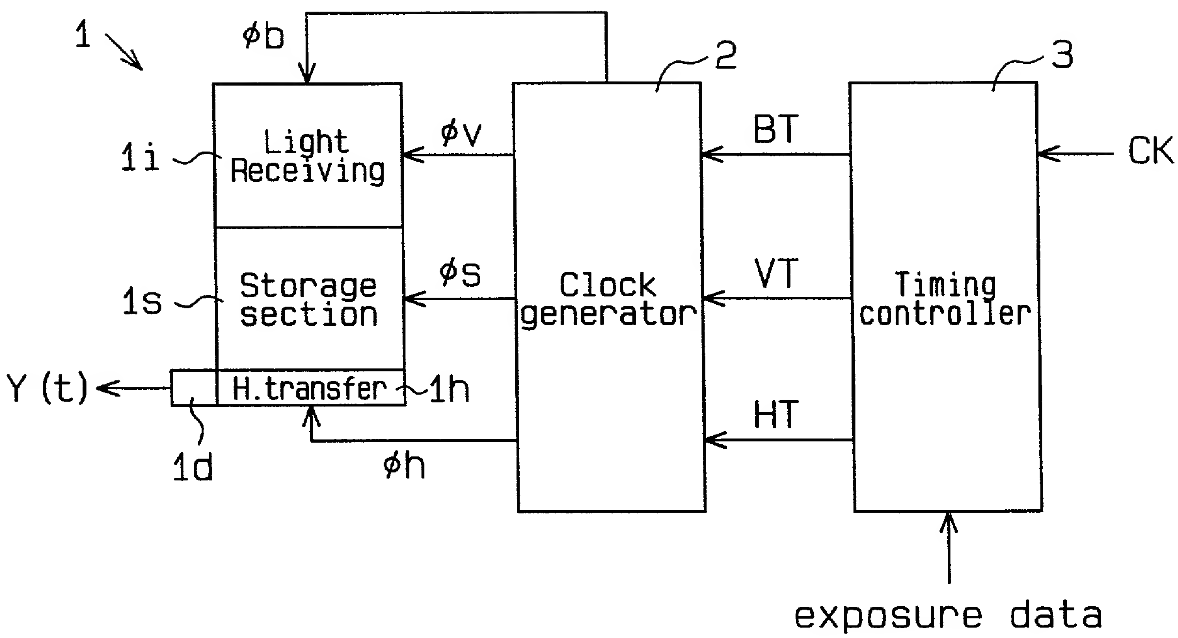


Fig.2 (Prior Art)

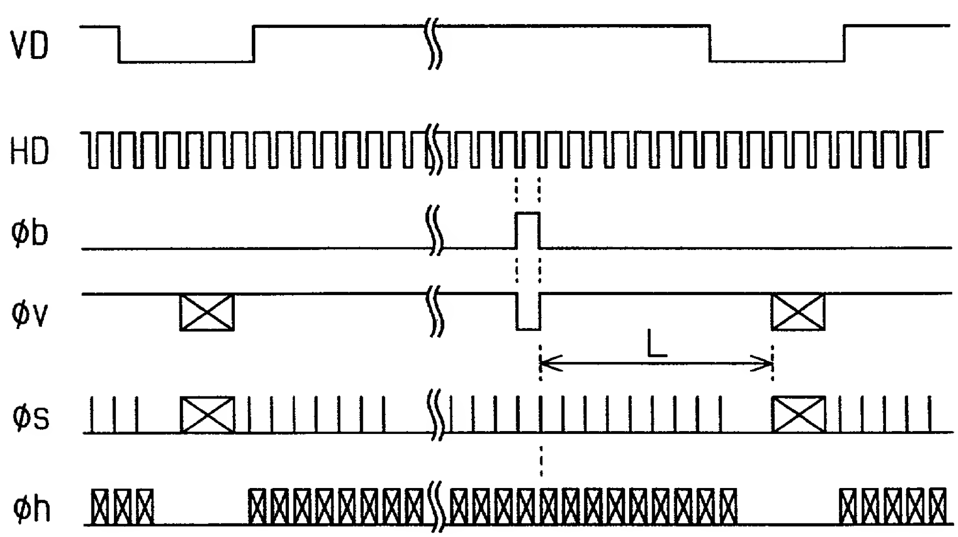


Fig.3(Prior Art)

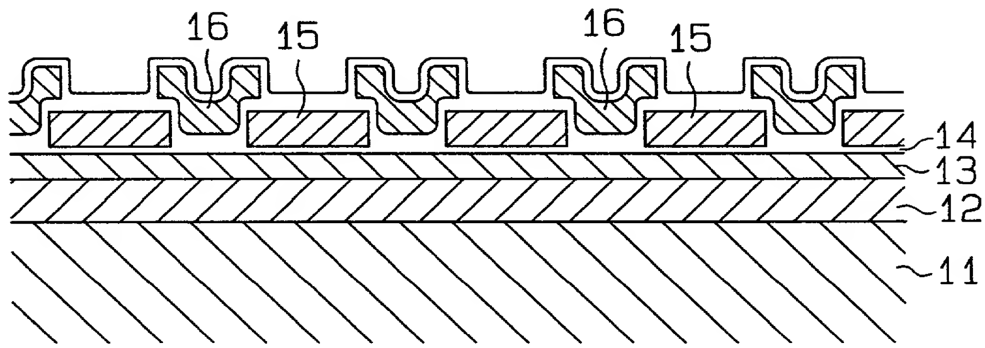


Fig.4(Prior Art)

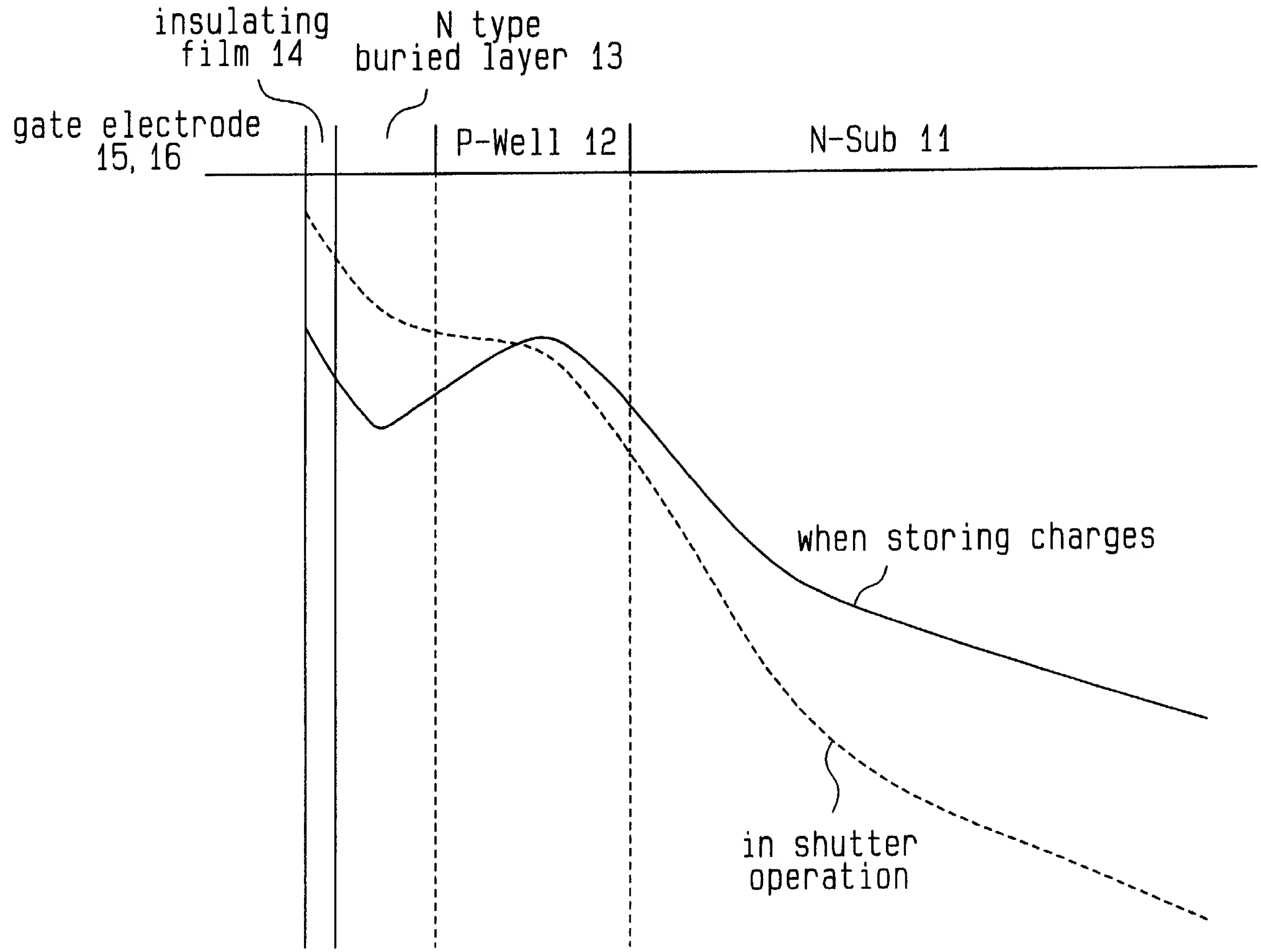


Fig.5

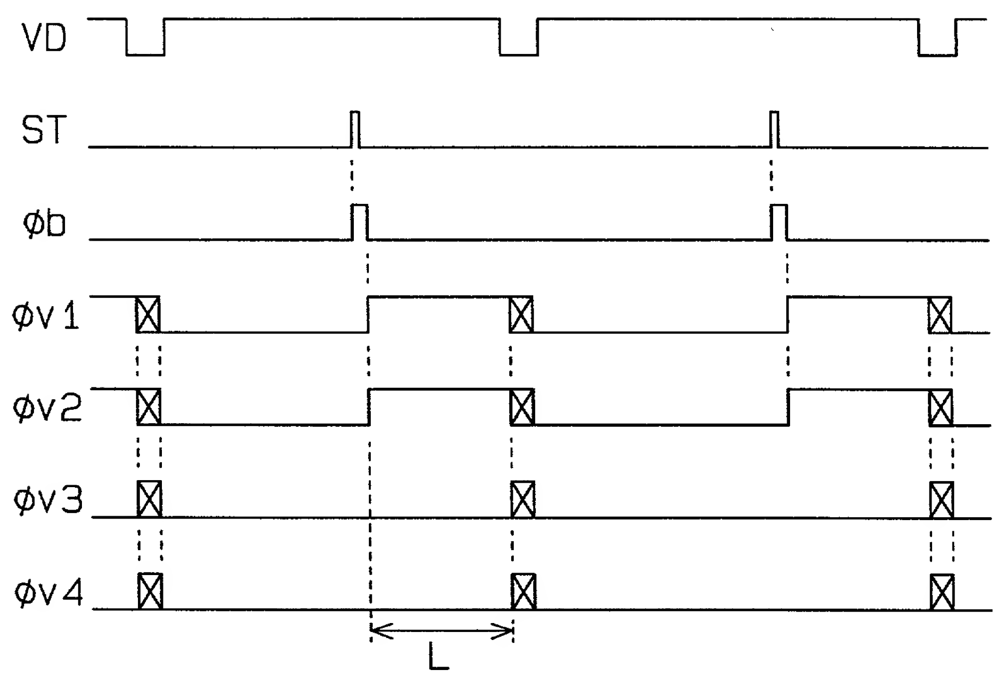
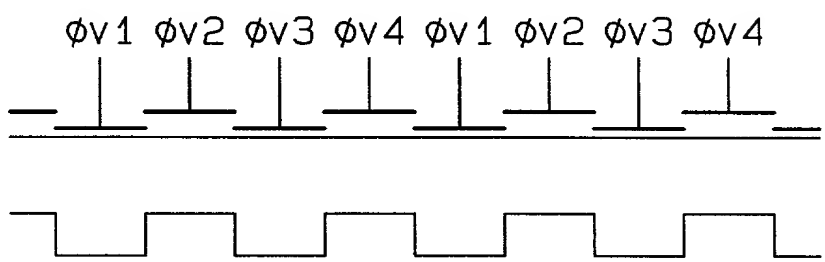
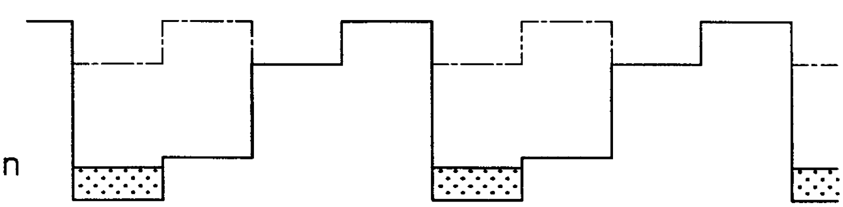


Fig.6A



From flame transfer completion to shutter operation completion

Fig.6B



From shutter operation completion to flame transfer completion

Fig.7

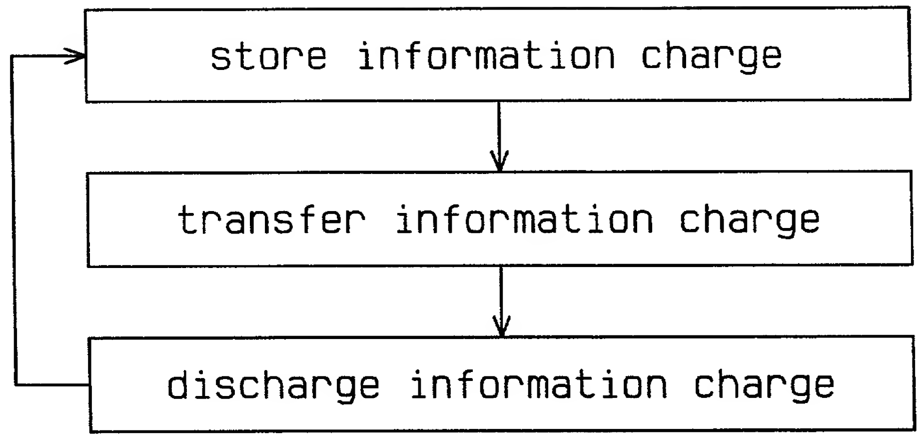
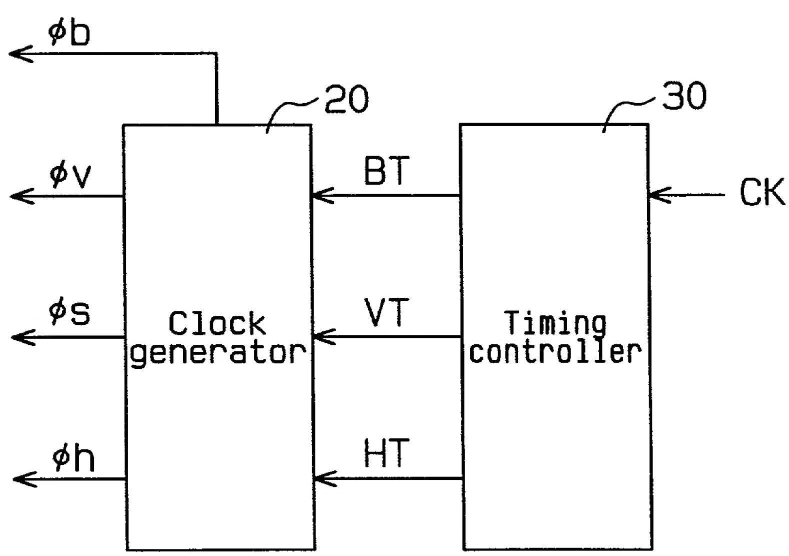

store information charge
transfer information charge
discharge information charge

Fig.8


φb
20
30
φv
BT
CK
φs
VT
Clock generator
Timing controller
φh
HT

Declaration and Power of Attorney For Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：	As a below named inventor, I hereby declare that:
私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、	My residence, post office address and citizenship are as stated below next to my name,
名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
__________	METHOD AND APPARATUS FOR DRIVING SOLID STATE IMAGE SENSOR
その明細書を (該当する方に印を付す)	the specification of which (check one)
☐ ここに添付する。	☒ is attached hereto.
☐ ________ 日に出願番号	☐ was filed on ________ as
第 ________ 号として提出し、	Application Serial No. ________
________ 日に補正した。 (該当する場合)	and was amended on ________. (if applicable)
私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。	I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
私は、連邦規則法典第37部第1章第56条（a）項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。	I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

			Priority claimed 優先権の主張	
Pat. Appln. No. 10-305820	Japan	27 / 10 / 1998	[X] Yes あり	[ ] No なし
(Number) (番　号)	(Country) (国　名)	(Day/Month/Year Filed) (出願の年月日)		
			[ ] Yes あり	[ ] No なし
(Number) (番　号)	(Country) (国　名)	(Day/Month/Year Filed) (出願の年月日)		
			[ ] Yes あり	[ ] No なし
(Number) (番　号)	(Country) (国　名)	(Day/Month/Year Filed) (出願の年月日)		

私は、合衆国法典第35部第120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112 条第１項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはＰＣＴ国際出願日の間に公表された連邦規則法典第37部第１章第56条（ａ）項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現　況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)
(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(現　況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。
（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*list name and registration number*)

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(Supply similar information and signature for third and subsequent joint inventors.)